



# RF Power Field Effect Transistors

## N-Channel Enhancement-Mode Lateral MOSFETs

Designed for PCN and PCS base station applications with frequencies from 1800 to 2000 MHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN-PCS/cellular radio and WLL applications. Specified for GSM 1805 - 1880 MHz.

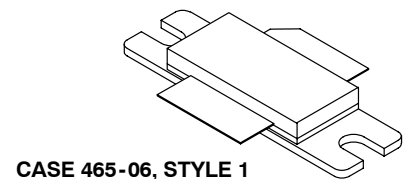
- Typical GSM Performance, Full Frequency Band (1805 - 1880 MHz)  
Power Gain — 13 dB @ 60 Watts  
Efficiency — 45% @ 60 Watts
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 1840 MHz, 60 Watts CW Output Power

### Features

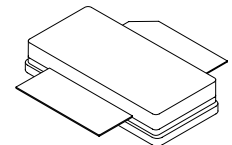
- Internally Matched for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Excellent Thermal Stability
- Available with Low Gold Plating Thickness on Leads. L Suffix Indicates 40μ" Nominal.
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 Inch Reel.

**MRF18060ALR3**  
**MRF18060ALSR3**

**1805-1880 MHz, 60 W, 26 V**  
**LATERAL N-CHANNEL**  
**RF POWER MOSFETs**



**CASE 465-06, STYLE 1**  
**NI-780**  
**MRF18060ALR3**



**CASE 465A-06, STYLE 1**  
**NI-780S**  
**MRF18060ALSR3**

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-0.5, +65	Vdc
Gate-Source Voltage	$V_{GS}$	-0.5, +15	Vdc
Total Device Dissipation @ $T_C \geq 25^\circ\text{C}$ Derate above 25°C	$P_D$	180 1.03	W W/°C
Storage Temperature Range	$T_{stg}$	- 65 to +150	°C
Case Operating Temperature	$T_C$	150	°C
Operating Junction Temperature	$T_J$	200	°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.97	°C/W

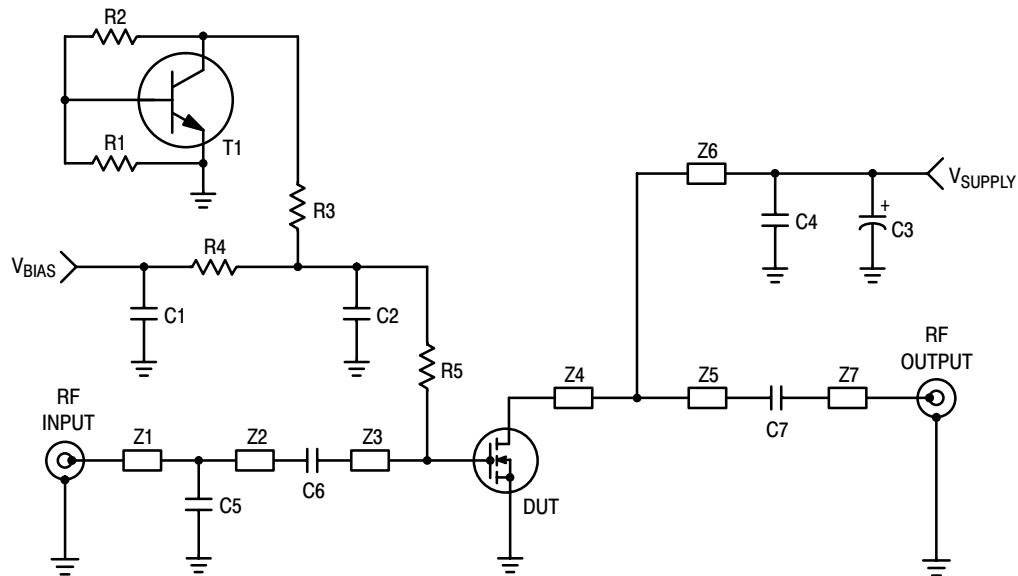
**Table 3. ESD Protection Characteristics**

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

**Table 4. Electrical Characteristics** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

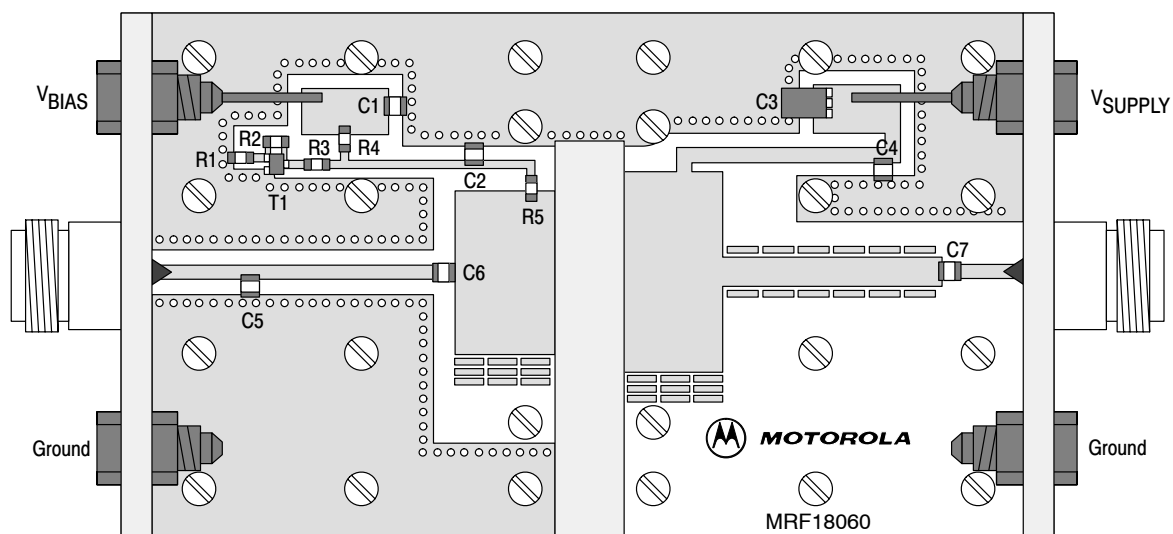
Characteristic	Symbol	Min	Typ	Max	Unit
<b>Off Characteristics</b>					
Drain-Source Breakdown Voltage ( $V_{GS} = 0\text{ Vdc}$ , $I_D = 10\ \mu\text{Adc}$ )	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current ( $V_{DS} = 26\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	6	$\mu\text{Adc}$
Gate-Source Leakage Current ( $V_{GS} = 5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	1	$\mu\text{Adc}$
<b>On Characteristics</b>					
Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 300\ \mu\text{Adc}$ )	$V_{GS(th)}$	2	—	4	Vdc
Gate Quiescent Voltage ( $V_{DS} = 26\text{ Vdc}$ , $I_D = 500\text{ mAdc}$ )	$V_{GS(Q)}$	2.5	3.9	4.5	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 2\text{ Adc}$ )	$V_{DS(on)}$	—	0.27	—	Vdc
<b>Dynamic Characteristics</b>					
Input Capacitance (Including Input Matching Capacitor in Package) (1) ( $V_{DS} = 26\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )	$C_{iss}$	—	160	—	pF
Output Capacitance (1) ( $V_{DS} = 26\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )	$C_{oss}$	—	740	—	pF
Reverse Transfer Capacitance ( $V_{DS} = 26\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )	$C_{rss}$	—	2.7	—	pF
<b>Functional Tests</b> (In Freescale Test Fixture, 50 ohm system)					
Common-Source Amplifier Power Gain @ 60 W (2) ( $V_{DD} = 26\text{ Vdc}$ , $I_{DQ} = 500\text{ mA}$ , $f = 1805 - 1880\text{ MHz}$ )	$G_{ps}$	11.5	13	—	dB
Drain Efficiency @ 60 W (2) ( $V_{DD} = 26\text{ Vdc}$ , $I_{DQ} = 500\text{ mA}$ , $f = 1805 - 1880\text{ MHz}$ )	$\eta$	43	45	—	%
Input Return Loss (2) ( $V_{DD} = 26\text{ Vdc}$ , $P_{out} = 60\text{ W CW}$ , $I_{DQ} = 500\text{ mA}$ , $f = 1805 - 1880\text{ MHz}$ )	IRL	—	—	- 10	dB

1. Part is internally matched both on input and output.
2. To meet application requirements, Freescale test fixtures have been designed to cover the full GSM1800 band, ensuring batch-to-batch consistency.



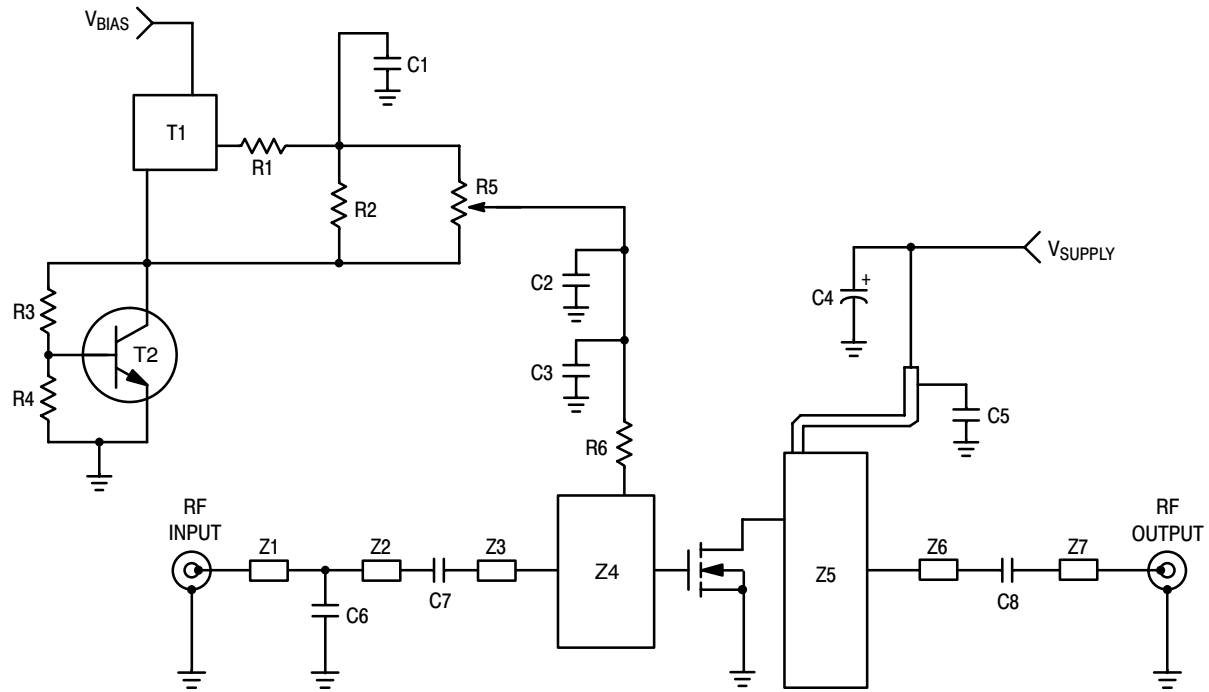
C1	100 nF Chip Capacitor (1203)	Z1	0.47" x 0.09" Microstrip
C2, C4, C7	10 pF Chip Capacitors	Z2	1.16" x 0.09" Microstrip
C3	10 $\mu$ F, 35 V Electrolytic Tantalum Capacitor	Z3	0.57" x 0.95" Microstrip
C5	1.2 pF Chip Capacitor	Z4	0.59" x 1.18" Microstrip
C6	1.0 pF Chip Capacitor	Z5	1.26" x 0.15" Microstrip
R1, R3	2.2 k $\Omega$ Chip Resistors (0805)	Z6	1.15" x 0.09" Microstrip
R2, R4	2.7 k $\Omega$ Chip Resistors (0805)	Z7	0.37" x 0.09" Microstrip
R5	1.1 k $\Omega$ Chip Resistor (0805)		
T1	BC847 Transistor SOT-23		

**Figure 1. 1805 - 1880 MHz Test Fixture Schematic**



Freescale has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescale Semiconductor signature/logo. PCBs may have either Motorola or Freescale markings during the transition period. These changes will have no impact on form, fit or function of the current product.

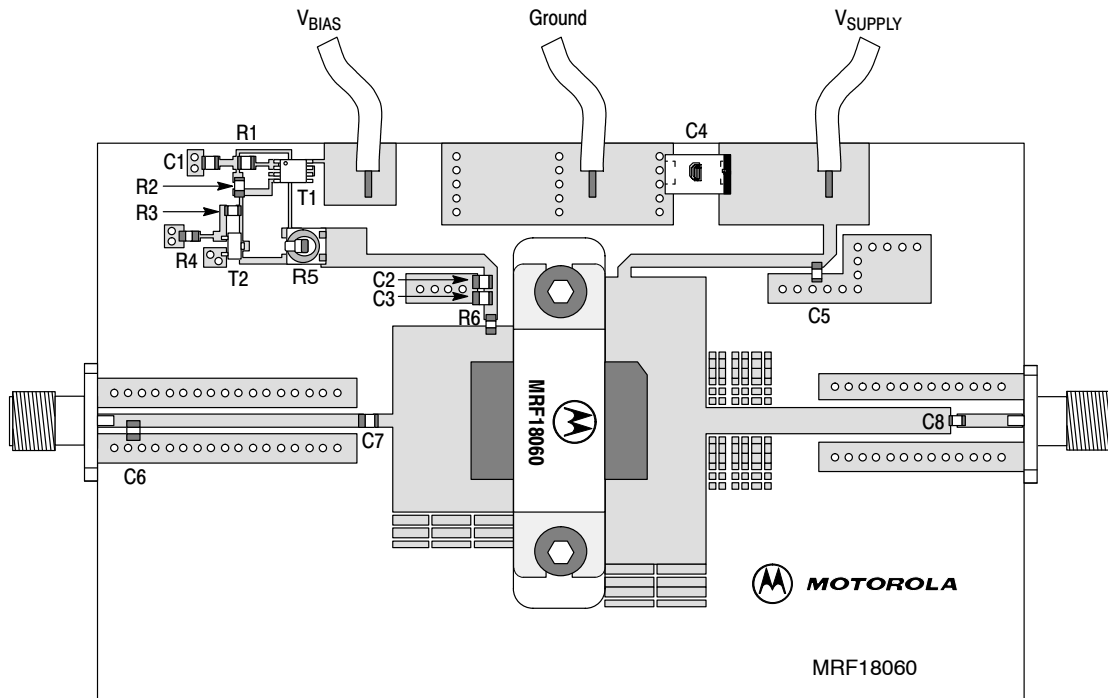
**Figure 2. 1805 - 1880 MHz Test Fixture Component Layout**



C1	1 $\mu$ F Chip Capacitor (0805)	T1	LP2951 Micro-8 Voltage Regulator
C2	100 nF Chip Capacitor (0805)	T2	BC847 SOT-23 NPN Transistor
C3, C5, C8	10 pF Chip Capacitors, ACCU-P (0805)	Z1	0.159" x 0.055" Microstrip
C4	10 $\mu$ F, 35 V Tantalum Electrolytic Capacitor	Z2	0.982" x 0.055" Microstrip
C6	1.8 pF Chip Capacitor, ACCU-P (0805)	Z3	0.087" x 0.055" Microstrip
C7	1 pF Chip Capacitor, ACCU-P (0805)	Z4	0.512" x 0.787" Microstrip
R1	10 $\Omega$ Chip Resistor (0805)	Z5	0.433" x 1.220" Microstrip
R2, R6	1 k $\Omega$ Chip Resistors (0805)	Z6	1.039" x 0.118" Microstrip
R3	1.2 k $\Omega$ Chip Resistor (0805)	Z7	0.268" x 0.055" Microstrip
R4	2.2 k $\Omega$ Chip Resistor (0805)		
R5	5 k $\Omega$ , SMD Potentiometer		

Substrate = 0.5 mm Teflon<sup>®</sup> Glass,  $\epsilon_r = 2.55$

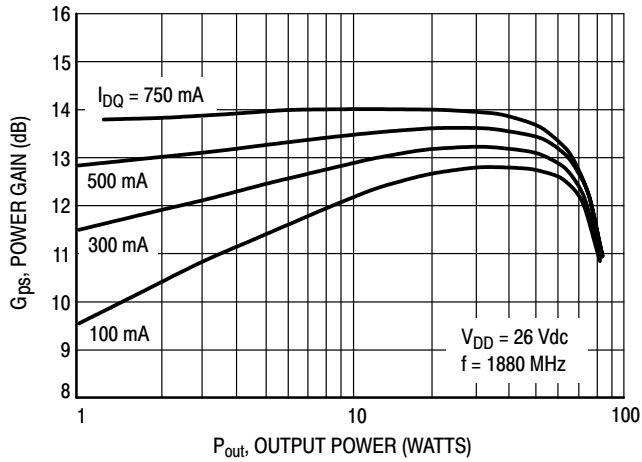
**Figure 3. 1800 - 2000 MHz Demo Board Schematic**



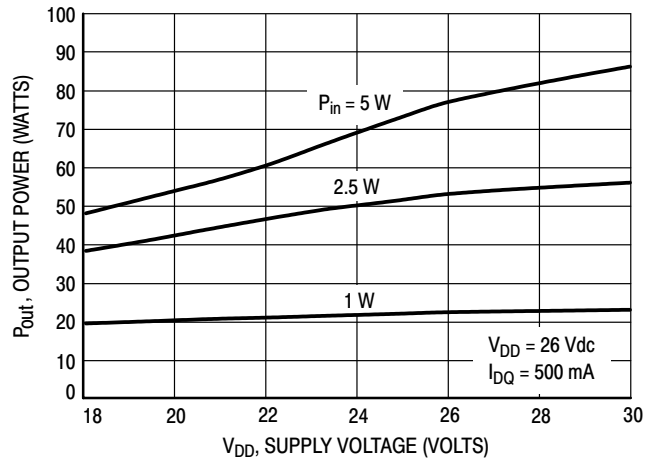
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**Figure 4. 1800 - 2000 MHz Demo Board Component Layout**

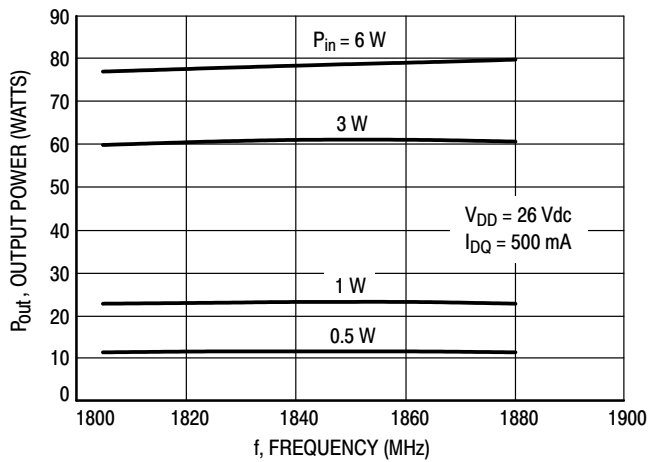
## TYPICAL CHARACTERISTICS (DATA TAKEN USING WIDEBAND DEMONSTRATION BOARD)



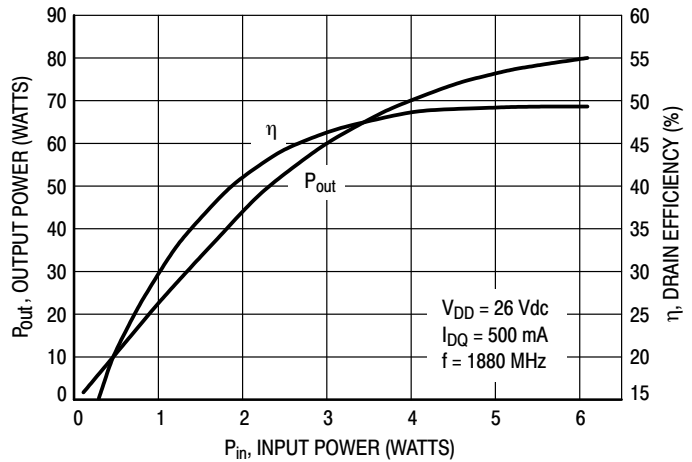
**Figure 5. Power Gain versus Output Power**



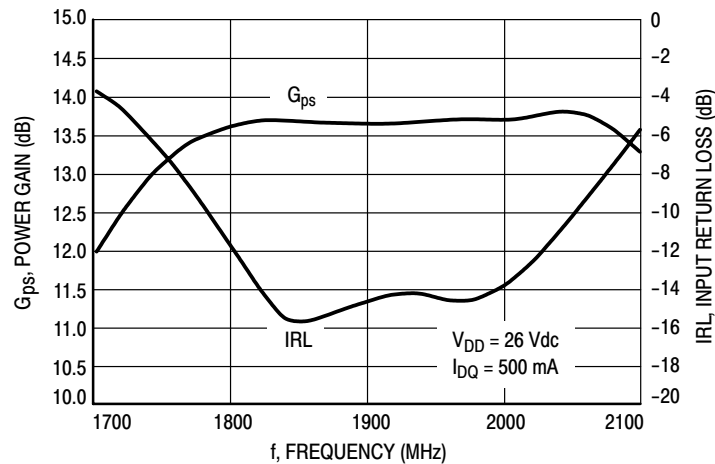
**Figure 6. Output Power versus Supply Voltage**



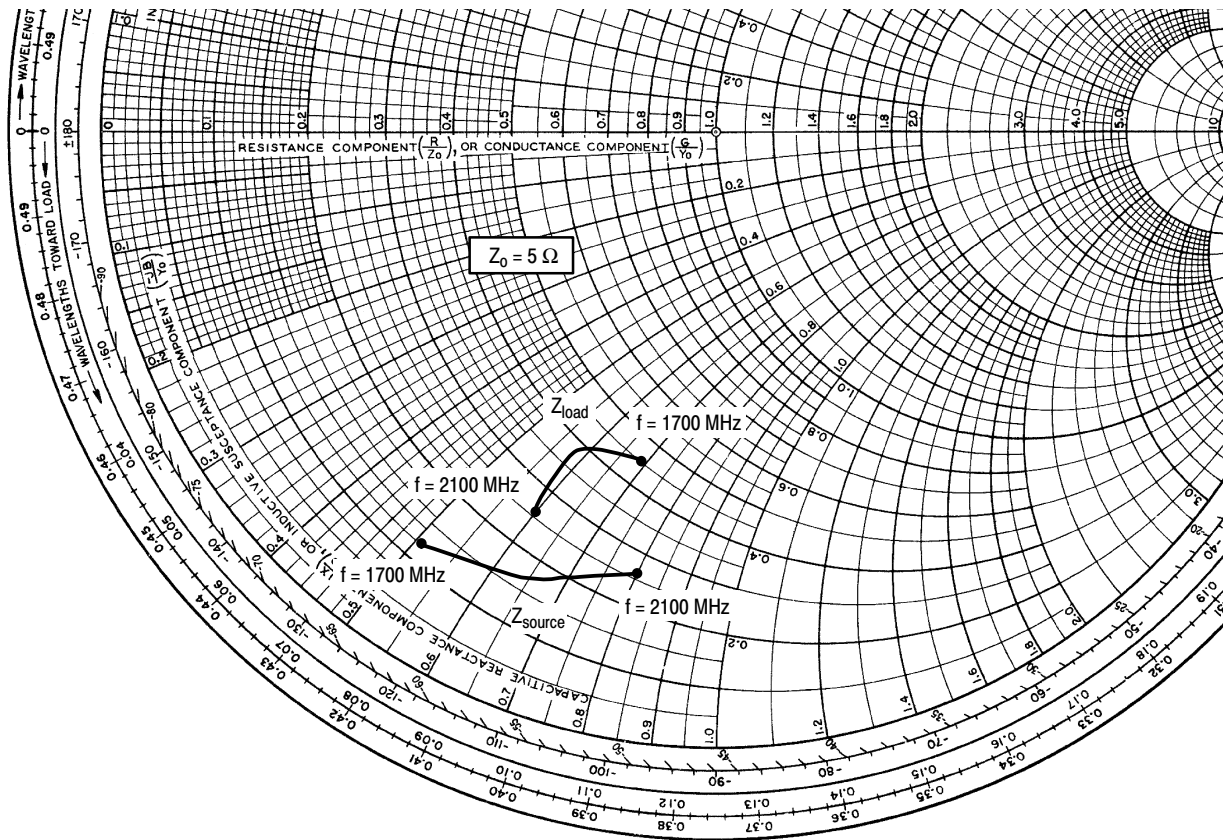
**Figure 7. Output Power versus Frequency**



**Figure 8. Output Power and Efficiency versus Input Power**



**Figure 9. Wideband Gain and IRL (at Small Signal)**



$V_{DD} = 26\text{ V}$ ,  $I_{DQ} = 500\text{ mA}$ ,  $P_{out} = 60\text{ W CW}$

f MHz	$Z_{source}$ $\Omega$	$Z_{load}$ $\Omega$
1700	$0.60 - j2.53$	$2.27 - j3.44$
1800	$0.80 - j3.20$	$2.05 - j3.05$
1900	$0.92 - j3.42$	$1.90 - j2.90$
2000	$1.07 - j3.59$	$1.64 - j2.88$
2100	$1.31 - j4.00$	$1.29 - j2.99$

$Z_{source}$  = Test circuit impedance as measured from gate to ground.

$Z_{load}$  = Test circuit impedance as measured from drain to ground.

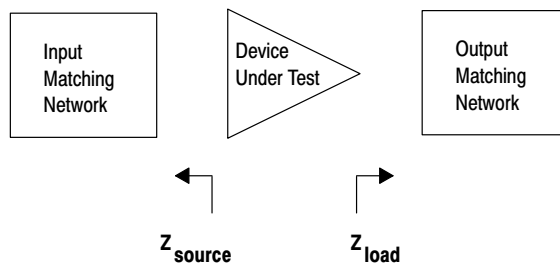


Figure 10. Series Equivalent Source and Load Impedance

# NOTES

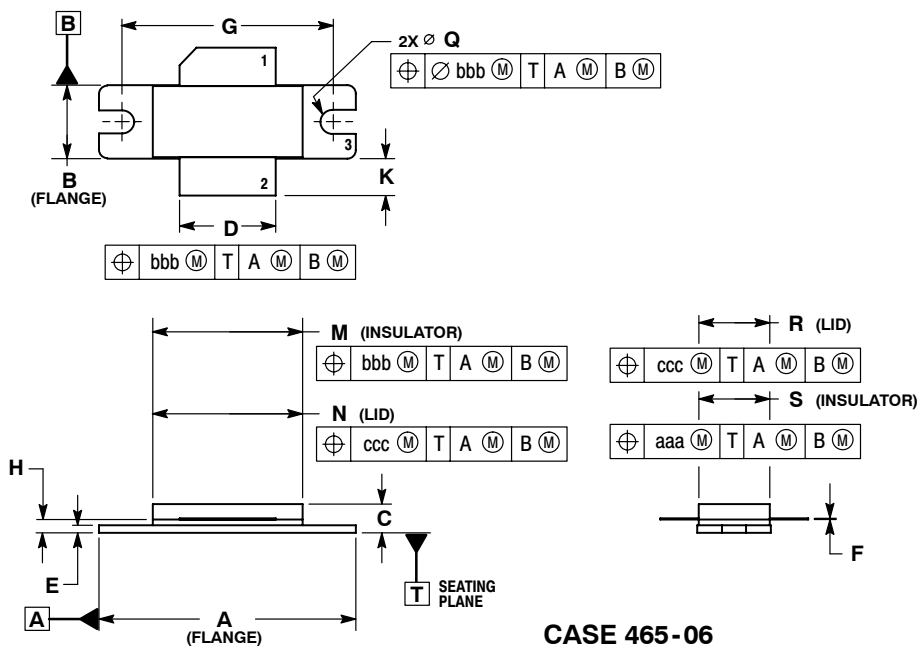




# NOTES

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## PACKAGE DIMENSIONS



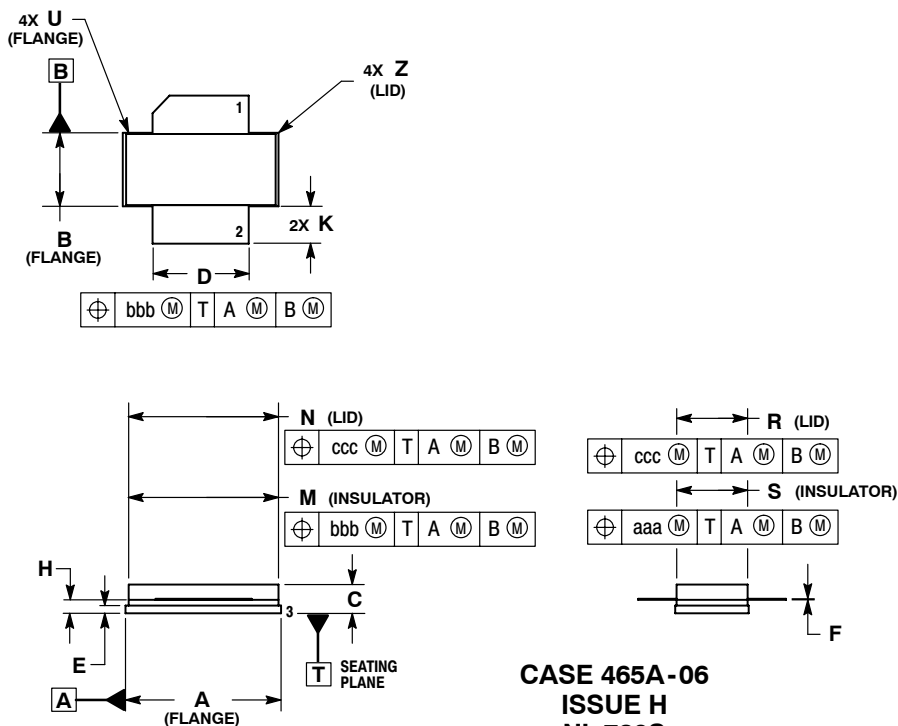
**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC 27.94 BSC			
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.66	19.96
N	0.772	0.788	19.60	20.00
Q	∅.118	∅.138	∅3.00	∅3.51
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

**STYLE 1:**

- PIN 1. DRAIN
2. GATE
3. SOURCE



**NOTES:**

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2. CONTROLLING DIMENSION: INCH.
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DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.805	0.815	20.45	20.70
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.61	20.02
N	0.772	0.788	19.61	20.02
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
U	---	0.040	---	1.02
Z	---	0.030	---	0.76
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

**STYLE 1:**

- PIN 1. DRAIN
2. GATE
5. SOURCE

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